

## SH-DSP

### One-chip multimedia age processor integrating DSP functions in SH core

SuperH has steadily evolved into the SH1, SH2, and SH3 series, and the SH4 Series is currently being deployed. Renesas has also released a roadmap for the SH5 and other next-generation series of the SuperH family. Particularly conspicuous among these SH series may be the SH-DSP Series. The SH2-DSP (SH7612), which mounts an SH2 core and DSP, and the SH3-DSP, which mounts an SH3 core and DSP, have been released, answering the needs of customers wanting to perform microcontroller and digital processing on one chip.

#### Answering chip reduction needs with CPU core + DSP functions

This new product was born as the result of market needs.

One approach often used for applications that require high-speed digital signal processing is to achieve higher processing speed through hardware-style methods such as the creation of ASICs. However, ASIC development involves high costs and takes a long time.

DSPs were developed as chips that can flexibly respond to changes through programming in order to realize high-speed processing in the particular field of digital signal processing. They employ a circuit configuration that allows high-speed processing of repetitive sum-of-products, and could be called dedicated digital signal processing microcomputers.

Though described as microcomputers, DSPs do not have the general versatility of CPUs and MPUs. They are simply tailored to digital signal processing. Generally the use of a DSP requires that a CPU as the main processor be also mounted at the same time, and this necessarily results in a 2-chip configuration.

A reduction in the number of chips that are used contributes to achieving a shorter TAT as well as lower cost, lower power consumption, equipment miniaturization, and so on. Ideally, SoCs would use a 1-chip configuration. SH-DSPs that combine the CPU core and DSP functions on one chip precisely answer this need for a reduction in the number of chips.

Currently, the SH-DSPs that have been released consist of the SH2-DSP (SH7612) combining an SH2 core + DSP, and the SH3-DSP (SH7729) combining an SH3 core + DSP.

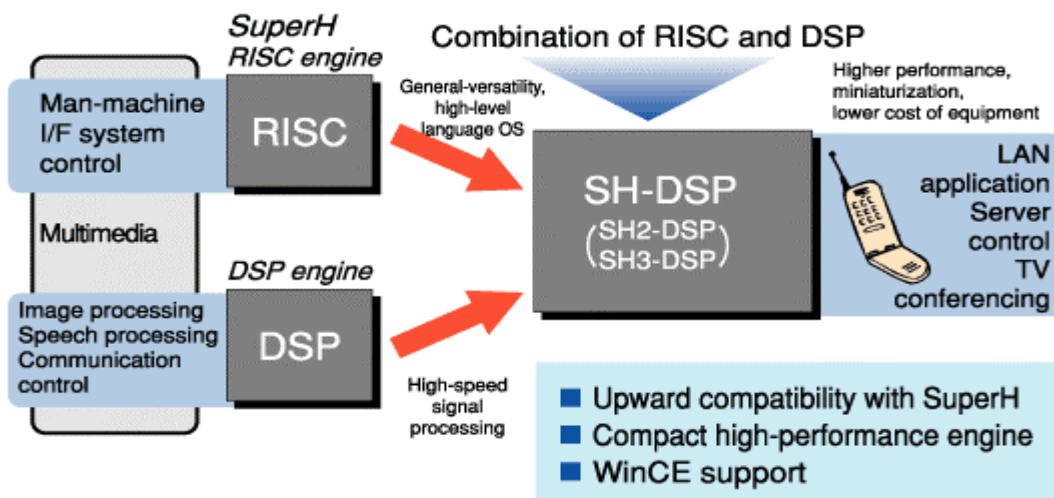


Fig. 1 SH3-DSP Development Concept

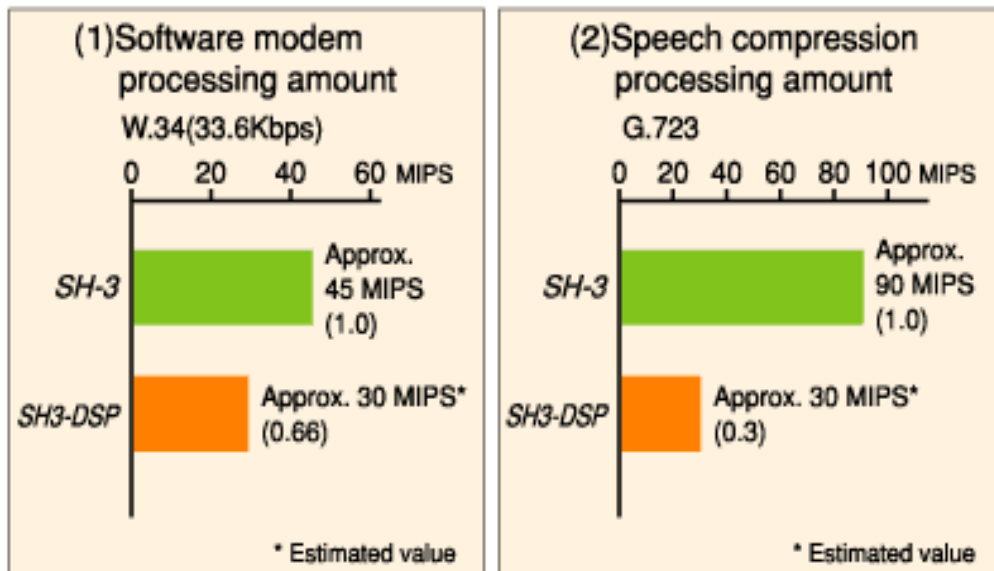


Fig. 2 Signal Processing Performance Example

### Expanding basic DSP functions provided by SuperH

SuperH originally had basic DSP functions such as sum-of-product. One of the features of SuperH is that it provides basic DSP such as sum-of-product, but Renesas expanded these basic DSP functions to enable full digital signal processing."

The SH2-DSP (SH7612), which consists of an SH2 core + DSP, offers sophisticated DSP operation functions such as single-cycle 16-bit by 16-bit signed multiplication, barrel shifting, priority encoding, rounding, modulo addressing, zero overhead, and loop control.

Multimedia processing is greatly improved by providing these DSP functions on chip. Figure 2 shows an example comparing the signal processing performance of the SH3-DSP and SH3.

The SH3-DSP can perform a given amount of V.34 (33.6 Kbps) shift modem processing in just 66% (estimated value) of the time it would take the SH3. Similarly, it can perform a given amount of G.723 speech compression processing in just 30% (estimated value) of the time required for the SH3.

This increase in processing speed is also clear in comparisons of the sum-of-product cycle. Figure 3 shows a comparison of the SH3 and SH3-DSP for sum-of-product operations using a 16-bit fixed point.

Use of the Harvard architecture in the SH3-DSP enables simultaneous access to the two internal X and Y memories in addition to the program code. As a result, the SH3-DSP can process sum-of-products in one cycle instead of two cycles as required by the SH-3.

### Suited for applications that require multimedia processing

By providing DSP functions on chip, the range of supported applications has been greatly expanded. The SH3-DSP is particularly suited for applications that require high-speed multimedia processing of the kind performed by the multimedia processing blocks of digital still cameras and digital video cameras, PDAs, handheld computers, and cellular phones.

For example, there is a high need for fast processing of Java applications for cellular phones such as PDCs. 384-Kbps data communication service are planned for

third-generation mobile phones. This thick bandwidth will enable the exchange of MPEG4 compressed moving pictures. In addition to baseband processing, such cellular phones will require a CPU for main control and a DSP for multimedia processing. SH-DSP is a processor ideally suited for processing other than baseband processing.

Moreover, lower power consumption, low cost, and other merits of SuperH will be preserved and stand to be exploited even more in digital home appliances, where cost competition is fierce, as well as mobile products, which require long battery-driven operation. Naturally, the combination of an SH core + DSP functions on one chip also has major merits for fax machines TV conferencing systems, cable modems and other stationary-type equipment, as well as applications for industry such as servo control.

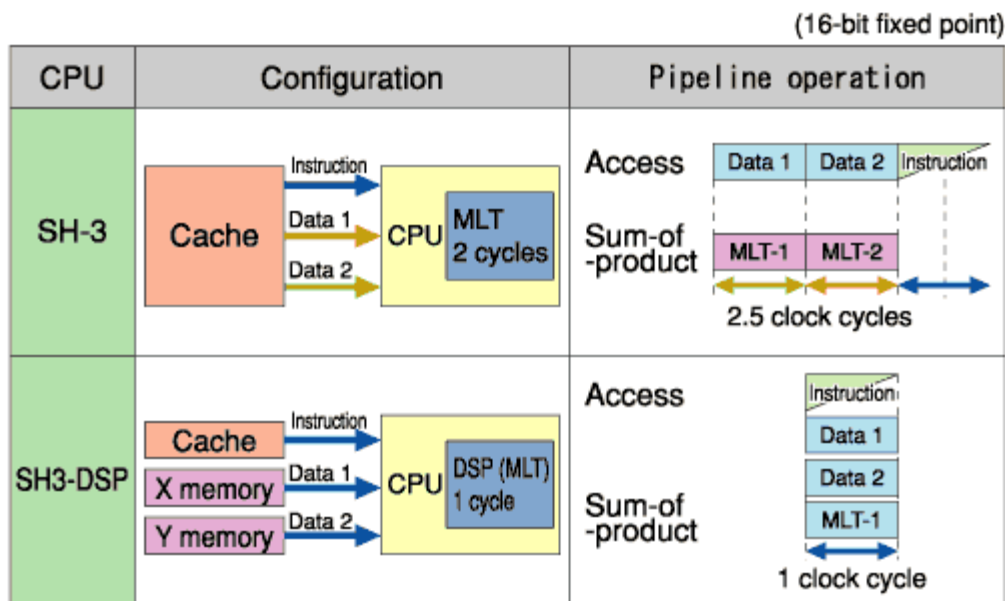


Fig. 3 Sum-of-Product Cycle Comparison

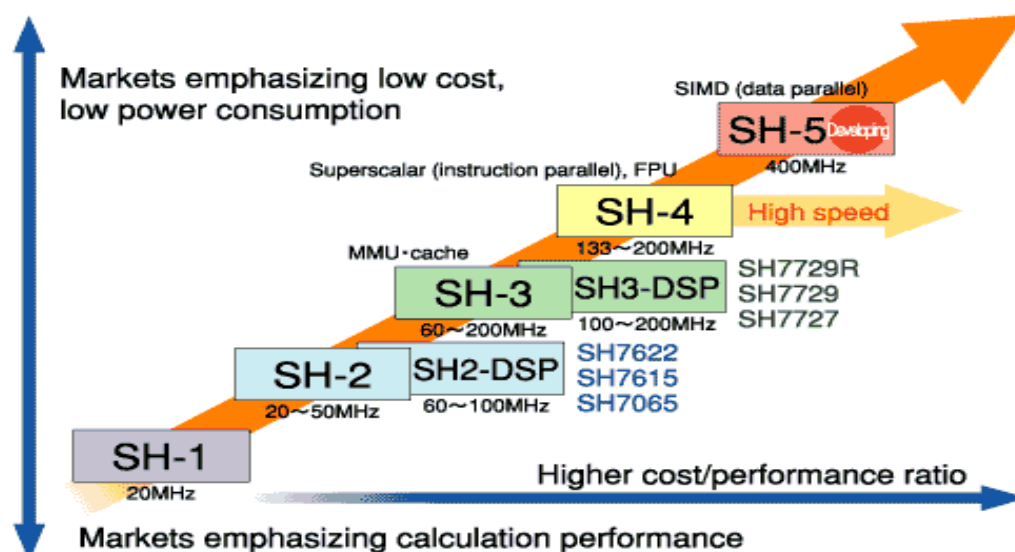


Fig. 4 Market and SH Microcontroller Core Markets

### **New compiler enabling DSP software development using C language**

A rich development environment is also available and a large array of development tools for SuperH can be used. These include Renesas-made tools as well as numerous third-party tools.

Hitachi-made tools

For example, Renesas has developed a compiler for SuperH that generates DSP code from C code, for use when performing upgrades. Since DSP software is generally written in assembler, development efficiency used to be low. This new compiler enables the development of DSP programs in C language by adding a DSP option.

Middleware offerings will also be expanded. The existing middleware library concentrates particularly on the field of cellular phones, including MPEG4, AAC, baseband interface, Java, and WAP. Renesas will now also increase the number of third parties who develop middleware for SH-DSP. Renesas' new compiler enabling the development of DSP programs even in C language is expected to lead to more middleware development by third parties.

Reference boards are indispensable for rapid development. Renesas Super LSI Systems and Renesas' Applied Development Department offer reference boards with SH-DSP. Some OS vendors also offer development kits consisting of SH-DSP boards to which they have ported their OS.

With regard to emulators, Renesas provides among other products the E10A PC card type on-chip debug emulator and the E-8000, a full ICE, and a number of third-party emulators are also available.

SH-DSPs are currently fabricated on the 76p platform, which uses a 0.18um process. creation of IPs is also being considered.

Regarding the SH3-DSP Series, work is being done to further lower power consumption. Chips that include memory are also being studied. Combining a CPU core, DSP functions, and memory on one chip will achieve a reduction in the number of external bus accesses, and result in lower power consumption and higher processing speed.

As multimedia processing is being required for various systems, the solutions offered by SH-DSP can be described as a perfect match for this age.